Correlated Degradation of Memory Window, Read Delay and Gate Leakage in Si Channel FEFETs Under Write Cycling

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Memory window, read-after-write delay (RWD) and gate leakage are three important device characteristics in Ferroelectric field effect transistors (FEFETs). While these parameters have been analyzed independently [1-3], a correlated understanding of the same is not present. In this work, we perform a comprehensive study of the evolution of these three characteristics under bipolar stress conditions (write cycling) and derive an understanding of trap generation and device behavior over the period of its lifetime. We track the I_D-V_G characteristics and gate leakage of a Si Channel FEFET with a 10 nm HZO layer under unipolar (without polarization switching) and bipolar stress (with polarization switching). The V_{th} shift in the low V_{th} state under bipolar and unipolar stress indicates increased trap generation when polarization switching is present.

We show that MW degradation and read delay are highly correlated. Traps leading to MW closure are primarily electron traps as evidenced by the significant positive shift in the low V_T state and minimal change in the high V_T state under bipolar stress (Fig. 1a). The evolution of MW recovery with read delay under bipolar cycling indicates that these traps are slow electron traps which eventually lead to the MW not being recoverable even with large read delay. Further, by comparing unipolar and bipolar cycling, we show that the slow electron trap generation is induced by polarization switching occurring during bipolar stress (Fig. 1b). The gate leakage does not change significantly until MW closure, indicating that these traps are localized mainly near the interfacial (IL) and do not contribute to trap assisted tunneling induced gate leakage. Beyond this initial degradation phase, a secondary mechanism emerges as the IL becomes increasingly damaged (Fig 2a). The redistribution of the internal electric field under these conditions leads to high electric field across the ferroelectric, triggering the formation of traps within the ferroelectric itself. These newly formed traps are responsible for the eventual rise in gate leakage current under bipolar stress.

Through this systematic experimental analysis, we establish a degradation pathway in FEFETs: polarization switching accelerates slow electron trap formation in the interfacial layer, which in turn drives both memory window closure and read delay increase. Once the IL is sufficiently degraded, trap generation shifts into the HZO bulk, leading to increased gate leakage. These findings emphasize the need to suppress slow-trap generation mechanisms in the IL, either by optimizing the interfacial layer properties or by employing cycling schemes that mitigate switching-induced stress. Such approaches are crucial to enhancing the long-term endurance and reliability of FEFETs in next-generation non-volatile memory applications.

References

[1] N. Gong et al., EDL 2017. [2] M Pešić et al., IRPS 2016. [4] M.Passlack et al., IEDM 2022.

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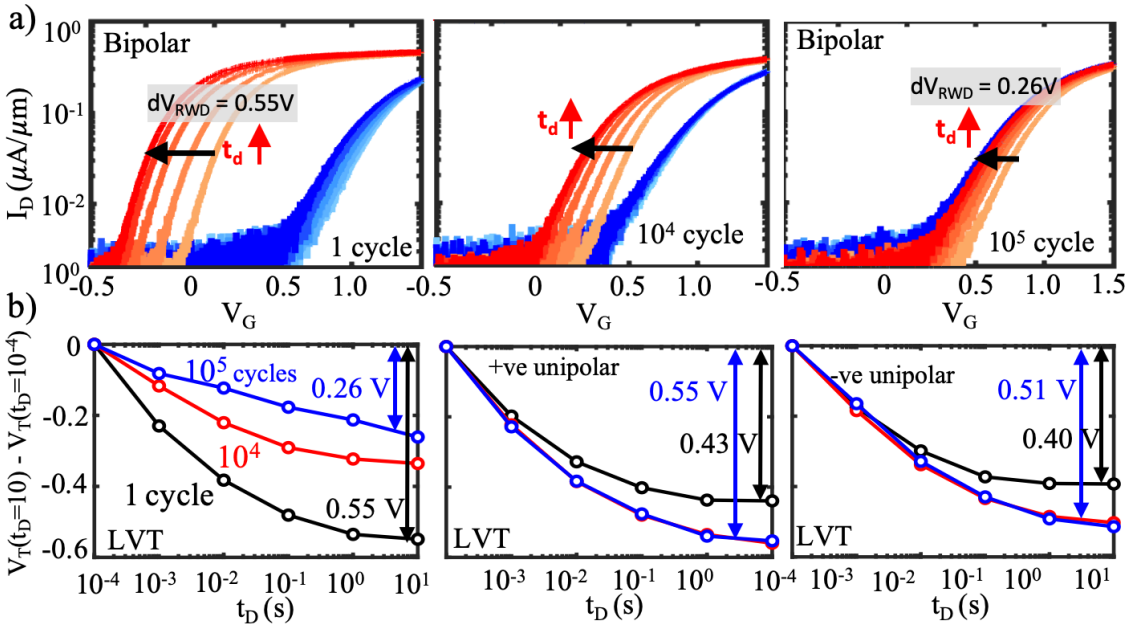

Figure 1: a) Measured Id-Vg curves for the different stress cases at each stage of cycling. As the device is cycled, the recovery of memory window with read delay (t_D) b) The shift in the Low V_T with stress cycles. Under bipolar stress, the Low V_T shifts significantly while the under unipolar stress the shift is minimal.

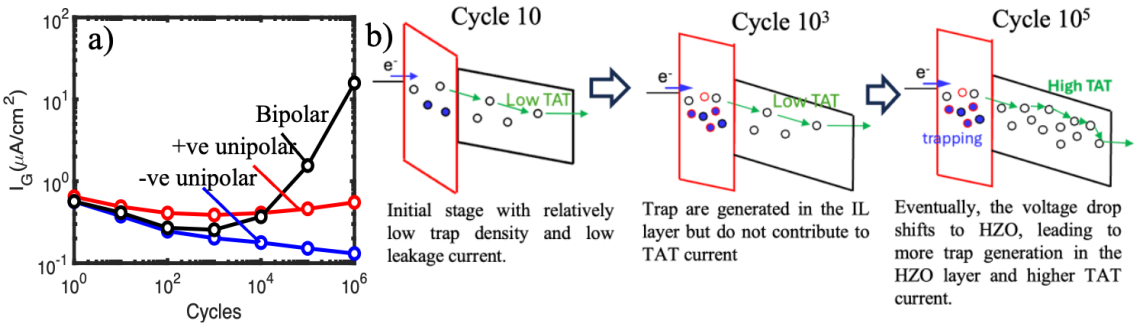

Figure 2: a) Gate leakage taken at -2.25V of a DC I_G-V_G characteristics vs stress cycles for all three stress cases. The leakage under bipolar stress stays under 1 μA/cm^2 until 10^4 cycles, then shoots up to 10 μA/cm^2 with subsequent cycling. b) Band diagrams show localized trap generation in the IL layer until memory window closure followed by trap generation in the FE layer leading to an increase in the gate leakage of the device.